maintaining the substrate at the first temperature, wherein the exposing step creates a first, uniformly thick, gate oxide film".

The Nayar article teaches a method of growing oxide layers. However, these oxides were not used as gate oxides. The article notes that the fixed oxide charges are high, and that the typical breakdown field is approximately 4 MV/cm. The Office Action implied that the GATE OXIDE CHARACTERISTICS NEEDED FOR SUBMICRON MOSFETS section of the Wolf, Vol. III lists characteristics that ordinary artisans would understand are necessary for/inherent in a conventional MOSFET gate oxide. Three of these characteristics are:

> 2. The specified oxide thickness must also be sufficiently uniform across the entire wafer, and from wafer to wafer, and from run-to-run.
> 3. The gate oxide film and the Si/SiO_2 interface must exhibit adequately small values of charge in the oxide and at the Si-SiO_2 interface. (i.e., low Q_f, D_{it}, Q_{ot} and Q_m values - see chap. 3).
> 4. The dielectric breakdown strength of the oxide must be sufficiently high (e.g., >8 MV/cm), implying that the film is pinhole free and contains a negligible number of defects that would lead to oxide breakdown at lower electric fields.[1]

The Nayar article explicitly teaches that its oxides have high fixed charges. Thus, ordinary artisans would understand that the Nayar article oxides would not be suitable for a conventional gate oxide. The Nayar article explicitly teaches that its oxides breakdown near 4 MV/cm. Thus, ordinary artisans would understand that the Nayar article oxides would not be suitable for a conventional gate oxide. The Nayar article does not mention that the oxide is highly uniform. Instead, the article mentions that the thickness measurements are averages. Additionally, an examination of the Nayar article fig. 2 shows that at 250° C, the oxide thickness may not be well behaved. Ordinary artisans would not be assured that the Nayar article oxides had sufficient thickness uniformity for a conventional gate oxide.

[1] Wolf, Vol. III, page 422.

In short, Applicants submit that an ordinary artisans would not consider an approach based on the Nayar article to have a reasonable expectation of success.[2] Without this expectation of success, obviousness has not been shown.

3. Applicants' claim 18 limitations also include the requirement that the gate oxide be uniformly thick. Nayar's useful method of forming extremely thick oxide layers at low temperatures makes no mention of obtaining uniform thicknesses. Instead, the Nayar article states that the thickness data is an average of several measurements[3]. Applicants submit that if Nayar had found high thickness uniformity (such as Applicants' <3% uniformity), the Nayar article would have reported the achievement. However, there is no evidence that the Nayar article's useful method creates uniformly thick layers—to which Applicants' claims are limited.

As Applicants understand it, the Office Action submits that uniformly thick layers would be an inherent property of a gate oxide. This may often be true. However, the Nayar article does not form gate oxides. Instead, it forms oxide films that are not suitable for use as gate oxides. Applicants submit that uniform thickness is not an inherent property of an ordinary oxide. Thus, again, the Office Action has not shown that ordinary artisans would have a reasonable expectation of success.

Applicants submit that the claims are patentable over the cited reference because the reference does not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of independent claim 18 and its dependants.

4. The Office Action rejected claim 1 under 35 U.S.C. § 103 as being unpatentable over Fujishiro '571 in combination with the Nayar article and Choquette *et al.* (Choquette '687).

Applicants arguments for claim 18 above are equally applicable to claim 1, and are repeated here by reference.

Claim 1's limitations also include "providing a partially completed integrated circuit on a semiconductor substrate with a clean, **atomically flat, silicon** surface". Choquette '687 teaches a useful process for removing surface contaminants such as C, Si and O, from substrates of the

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[2] "Obviousness does not require absolute predictability, but a reasonable expectation of success is necessary." -- In Re Clinton, 188 U.S.P.Q. 365 (CCPA, 1976).

[3] See p. 206, line 3.

gallium arsenide or indium phosphide families. Applicants have studied Choquette '687—including the abstract section cited—and have not found where it teaches a method of forming an atomically flat Si surface. The abstract does mention that this method forms an atomically smooth semiconductor surface. However, when read in context with the rest of the disclosure, Applicants submit that Choquette '687 enables forming atomically smooth surfaces on III-IV semiconductors, such as gallium arsenide, indium phosphide, and the like. Applicants submit that ordinary artisans would not expect a method to remove Si from a GaAs surface would be useful to form the claimed atomically flat, silicon surface. As such, obviousness has not been established.

Applicants also disagree with Examiner's assertion that ordinary artisans would be clearly motivated to provide an atomically flat surface.

Applicants submit that the claims are patentable over the cited reference because the reference does not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of independent claim 1 and its dependents.

5. Applicants believe that the application is in condition for allowance. If Examiner has any further comments or suggestions, Applicants respectfully request that Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Respectfully submitted,

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